skylabs

NANOobc Gen2 (nano-obc-2)

NANOobc Gen2 Interface Control Document

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Approval of Document

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Revision history

Last Edited Date	Revision Number	Status	Edited By	Paragraphs Affected	Change Ref
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30/10/2019	1.0	Draft	DGA	All	Review and Minor Changes
27/11/2019	1.1	Draft	DGA	S 2.3	Added GPS receiver details
28/02/2020	1.2	Draft	DSE	S 4, S 6	Updated pinout, GPIO specifications, minor typo fixes
30/03/2020	1.3	Draft	DSE	S 3	Added mechanical diagrams and locations of temperature sensors
09/04/2020	1.4	Draft	DSE	S 4.1.1	Added mechanical diagrams and locations of temperature sensors
11/05/2020	1.5	Draft	DSE	S 3.4	Added grounding scheme
03/07/2020	1.6	Draft	DSE	S 4.1.1	Explicitly labelled GPIO pins
22/07/2020	1.7	Draft	DSE	S 4.1.1 S 6	Updated connector descriptions. Added interface schematics.
30/09/2020	1.8	Draft	DSE	S 4.1.1	Synchronized CAN bus names across SkyLabs product lines, added explicit reference to nominal/redundant bus.
08/01/2021	1.9	Draft	DSE	S 3.3	Expanded inrush current chapter. Refined power consumption figures.
27/01/2021	1.10	Draft	NFE	S 3.7	Updated technical drawing and mechanical envelope
12/02/2021	1.11	Draft	NFE	S 2.3, S3.7	Updated mass, technical drawing and centre of mass.
02/02/2021	1.12	Release	DGA	S 2.3	Consolidated technical specifications
25/03/2021	1.13	Release	DGA		Features list consolidated

02/04/2021	1.14	Release	NFE	S 3.8	Updated centre of mass and added MoI.
13/01/2022	1.15	Release	DGA	S1	Updated image

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1 Introduction

1.1 Scope

The following document provides the Interface Control Document for the NANOobc Gen 2 (nano-obc-2), from hereinafter NANOobc.

1.2 Applicable Documents

Applicable Documents identified in the following text are identified by AD-n, where “n” indicates the actual document, from the following list:

AD#	Title	Doc. No.	Issue	Date
AD1				

1.3 Reference Documents

Documents referenced in the following text, are identified by RD-n, where “n” indicates the actual document, from the following list:

RD#	Title	Doc. No.	Issue	Date
RD1	ROAD VEHICLES -- CONTROLLER AREA NETWORK (CAN) - PART 1: DATA LINK LAYER AND PHYSICAL SIGNALLING.	ISO Standard-11898-1		2013
RD2	PC/104-Plus Specification		Version 2.3	October 13, 2008

1.4 Acronyms and Abbreviations

AD	Applicable Documents
AR	Acceptance Review
BM	Breadboard Model
CCSDS	Consultative Committee for Space Data Systems
CDR	Critical Design Review
CLI	Command Line Interface
CoG	Centre of Gravity
COP	Communications Operations Procedure
CSP	Cost, Schedule, Performance
CTIA	Capacitive Trans Impedance Amplifier
DDJF	Design Development and Justification File
DDVP	Design Description and Verification Plan
EM	Engineering Model
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EQM	Engineering Qualification Model
FARM	Frame Acceptance and Reporting Mechanism
FOV	Field of view

FS	Feasibility study
FWHM	Full Width at Half Maximum
IC	Integrated Circuit
ICU	Interface and Control Unit
ICD	Interface Control Document
JTAG	Joint Test Action Group
LEO	Low Earth Orbit
NIY	Not Implemented Yet
NVM	Non-Volatile Memory
PDR	Preliminary Design Review
PFM	Proto Flight Model
PRR	Preliminary Requirements Review
RD	Reference Documents
OBC	On-Board Computer
QM	Qualification Model
QR	Qualification Review
SNR	Signal to Noise Ratio
SPU	SDR Processing Unit
SRR	System Requirements Review
TBC	To Be Confirmed
TBD	To Be Determined
TBM	Test Bench Model
TOA	Time of Arrival
UART	Universal Asynchronous Receiver/Transmitter
WBS	Work Breakdown Structure
WP	Work Package

2 NANOobc Overview

The NANOobc on-board computer represents the newcomer in the emerging space market. Its fault tolerance by design provides remarkable reliability and robustness against SEE. Fault tolerance is assured by redundancy on the component level and their flight heritage, latch-up protection by constant current monitoring and several mitigation techniques. The NANOobc is powered by PicoSkyFT processor, which furthermore increases operational reliability and delivers nearly 16 MIPS. NANOobc features a redundant mass storage and sufficient capacity of non-volatile and volatile program and data memories to assure functionality for the most demanding space applications.

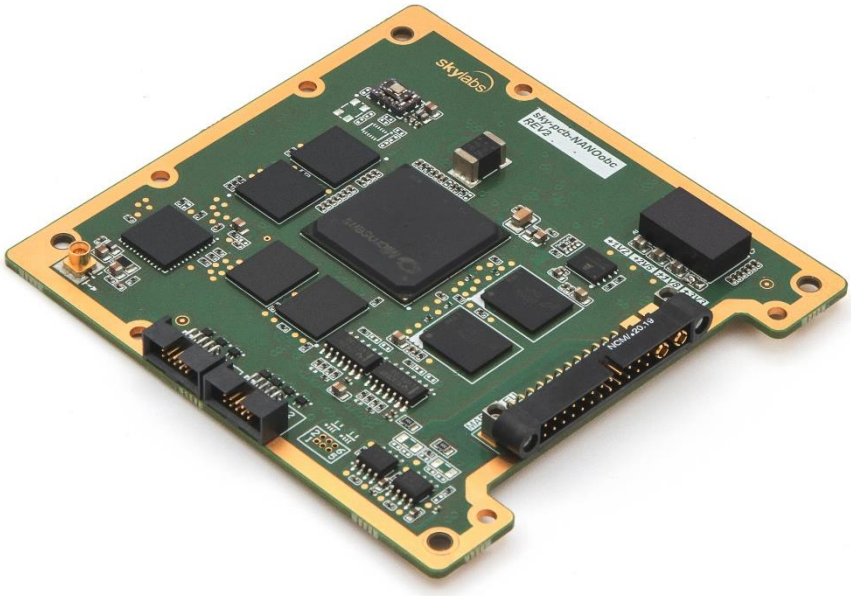

Figure 1: NANOobc (nano-obc-2)

2.1 Features

- Radiation hardened by design to increase reliability and robustness
  - Constant current monitoring and limiting
  - Selective components technology selection with flight heritage
  - EDAC protected memories/registers
  - Advance FDIR techniques
- SoC powered by fault tolerant PicoSkyFT processor
- Redundant mass storage NAND Flash with capacity of 2 GB
- SEE immune non-volatile MRAM memories for code and TM storage
- Instant boot up at power on
- Comprehensive local subsystem telemetry (currents, voltages, temperatures, etc.)
- Interfaces:
  - Dual LVDS interface links for high-speed data transfer (EIA/TIA-644)
  - Hot/cold redundant CAN interface for TM/TC
  - 8 GPIOs with interface remapping capability (SPI, I2C, UART, 1PPS)
  - PicoSkyFT™ programming and debugging interface
- GNSS receiver with 1 PPS signal output capability
  - Receiver type: L1 C/A code, GPS QZSS, 167 channels
  - Position accuracy: 2.5m CEP
  - Velocity accuracy: 0.1m/sec
  - Timing accuracy: 10ns
  - Open sky TTFF: 29 second cold start, 1 second hot start, reacquisition < 1s
  - Operational limits: Velocity 10Km/s+

2.2 Architecture overview

The NANOobc hardware architecture is designed around the use of a PicoSkyFT softcore inside an IGLOO2 FPGA. The hardware includes two parallel MRAM memories (total of 4 Mbytes) for use as the program memory as well as two parallel SRAM memories (total of 2 Mbytes) for use as the data memory of the PicoSky core. Additionally, two NAND Flash memories (total of 2 Gbytes) function as a mass storage memory for various user data. Further, a SPI MRAM (total of 1 Mbyte) is present for storing critical system logs and other telemetry.

The NANOobc exposes two different interfaces. First, two CAN drivers support interfacing the NANOobc to a redundant CAN bus. Additionally, two high-speed LVDS links are supported. The NANOobc supports the monitoring of local telemetry through on-board ADCs. A debug connector compliant with the PicoSkyLINK is also present, exposing local debugging functionality. The PicoSkyFT SoC is clocked at 16 MHz.

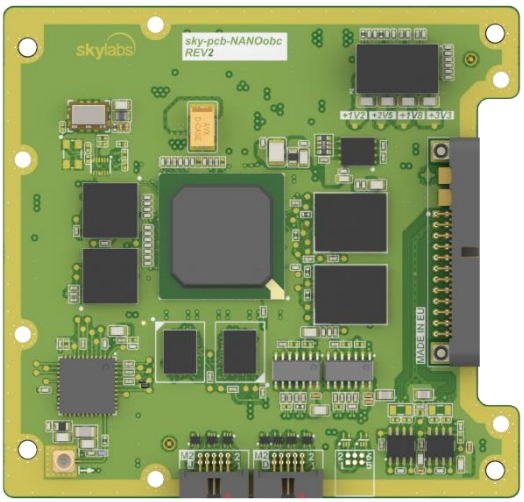

Figure 2: NANOobc - Top

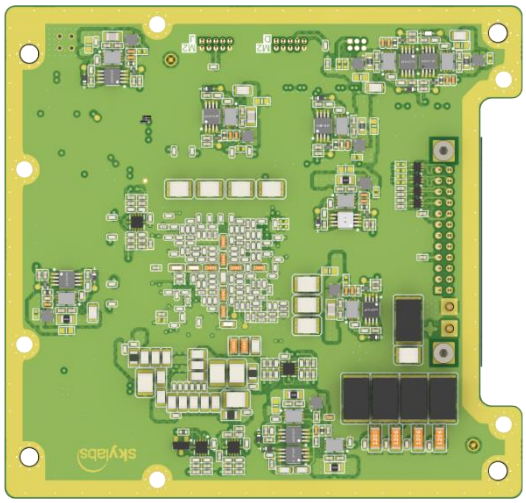

Figure 3: NANOobc - Bottom

2.3 Technical specifications

Table 1: NANOobc (nano-obc-2) - Technical specification

	Description	Comment
Processor	PicoSkyFT SoC, running at 16MHz	
On board memories		
Code memory	MRAM 4 MB (1Mb x 32-bit, unlimited read/write endurance, SEE immune)	EDAC protected
Data memory	SRAM 2 MB (1 Mb x 16-bit)	EDAC protected
TM storage	Serial MRAM 4 Mb (unlimited read/write endurance, SEE immune)	EDAC protected
Mass storage	2 GB	High speed hot redundant NAND Flash (EDAC protected)
On-board Communication interfaces	Redundant CAN bus Redundant High speed LVDS 8 GPIOs with remap capability	 Possibility to use as UART, I2C, SPI, 1PPS output, or trigger output. Also optional in differential configurations for 2 IOs.
On-board GPS receiver		
Receiver Type	L1 C/A code GPS QZSS 167 channels	
Accuracy	Position 2.5m CEP Velocity 0.1m/sec Timing 10ns	
Open sky TTFF	29 second cold start 1 second hot start	
Reacquisition	< 1s	
Sensitivity	-165dBm tracking -148dBm cold start	
Update Rate	1 / 2 / 4 / 5 / 8 / 10 / 20 / 25 / 40 / 50 Hz	(default 1Hz)
Dynamics	4G	
Operational Limits	Velocity 10Km/s+	
Datum Default	WGS-84	
Baud Rate	4800 / 9600 / 38400 / 115200	
Protocol	NMEA-0183 V3.01, GGA, GLL, GSA, GSV, RMC, VTG, ZDA	
Supply voltage	5 V DC (+/- 10%)	For details please refer to section 3.3.
Power consumption	< 1 W (peek) < 0.9 W (idle mode)	For details please refer to section 3.3.

Dimensions:	95 x 91 x 11 mm	For detail refer to section 3.7.
Operation temperature	-10°C to +60°C	For details refer to section 3.9.1.
Storage temperature	-20°C to +65°C	For details refer to section 3.9.1.
Mass:	55 g	For details refer to section 3.8.

3 Module specifications and generic parameters

3.1 Primary Function and Description

The NANOobc is designed to function as the primary on-board computer of a nanosatellite. As such, it implements a PicoSkyFT core with sufficient amounts of program and data memory for even the most intensive tasks, while being compatible with the PC-104 form factor. It supports a hot redundant CAN bus interface as well as two high-speed LVDS interfaces, supporting the 10b8b coding scheme. It features extensive fault tolerant features, including the features built into the FT version of the PicoSkyFT core, as well as integrated Latching Current Limiters and additional SoC protections (Watchdog timer, two CRC protected banks of program memory).

The NANOobc system contains:

- IGLOO2 FPGA running PicoSkyFT.
- Protection of FPGA, power regulator and related circuitry by autonomous LCL.
- 2 x 16x1M MRAM as program memory (protected by LCL).
- 2 x 8x1M SRAM as data memory (protected by LCL).
- 2 x 1GB NAND Flash (protected by LCL).
- 4 Mbit SPI MRAM (protected by LCL).
- Redundant CAN interface (PHYs protected by individually LCL).
- 2 x high speed LVDS interface (protected by LCL).
- Debug interface.
- Local telemetry monitoring (Voltages, Temperatures).
- GNSS receiver with 1 PPS signal

The PicoSkyFT SoC design includes:

- PicoSkyFT core running at 16 MHz.
- LUT-based supervisor for protecting user program from errors.
- LUT-based program memory CRC check assuring valid code is running.
- A two-bank program memory architecture, allowing the running program to perform upgrades to the firmware in the other bank.
- Multi-channel DMA controller
- Timers
- UART controller
- SPI-MRAM NVMEM controller with EDAC support
- CAN controller
- ONFI compliant NAND controller
- LCL management peripheral with error injection capability.
- Multichannel ADC controller
- LVDS controllers
- Watchdog timer
- On-Boar Time controller with PPS signal distribution and fail over to synthetic PPS in case of lost GNSS

3.2 Module Block Diagram

The NANOobc design is focused that most hardware components are accessed using a dedicated SoC peripheral. The exceptions are the MRAM and SRAM memories, which are connected directly to the PicoSky core. The following block diagram demonstrates the NANOobc design.

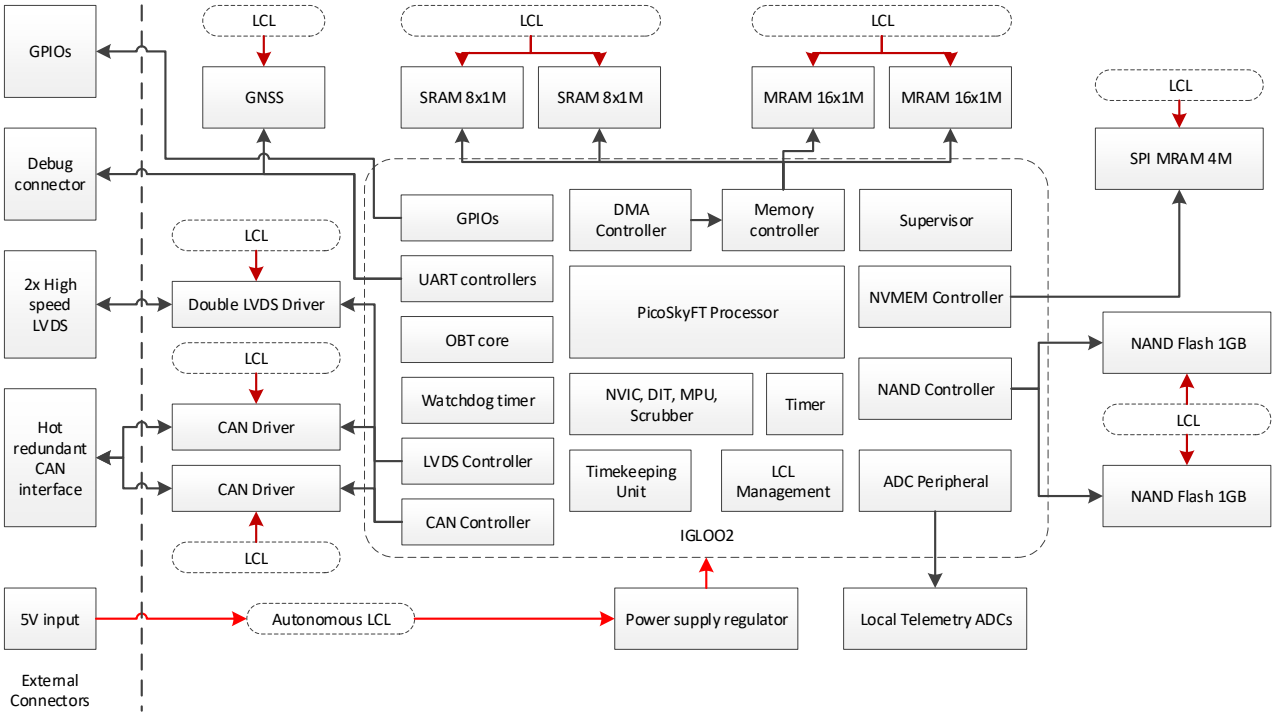

Figure 4: NANOobc Basic block diagram

3.3 Electrical Power

NANOobc shall be powered with 5V regulated power line. Other required NANOobc voltages are generated internally with integrated DC-DC converters. Associated voltage ranges are 1.2V, 1.8V, 2.5V, 3.3V and 5V.

Values are given for one NANOobc.

Table 2: NANOobc Electrical characteristics

Num. of power interfaces:	1 (5 V, ±10%)
Voltage rails:	1.2 V, 1.8 V, 2.5 V, 3.3 V, 5 V

Table 3: NANOobc Power consumption

Power consumption	At 25 °C	At -35 °C	At 70 °C
Idle mode • All CAN channels terminated. • GNSS active, no antenna connected	0.86 W	0.83 W	0.95 W
Active mode • All CAN channels terminated. • GNSS active, no antenna connected • LVDS, MRAM and NAND active	0.87 W	0.84 W	0.99 W

3.3.1 Inrush current profile

The inrush current of the NANOobc is defined by the input capacitances of the NANOobc local power supply DC-DC converters. There is no active inrush limiting circuitry present on the NANOobc.

Table 4: NANOobc Inrush current characteristics

Equivalent input capacitance	140 uF
Inrush profile (lead connected to 5V power supply, no soft start): • Inrush duration • Inrush peak	 40 us 25 A
Inrush charge transferred (0V to 5V)	0.70 mAs

3.3.2 Turn off/on procedure

The on/off procedure of NANOobc is to switch on/off its power supply line and/or via on-board subsystem LCL where in case of a detected anomaly (excessive current draw) resets autonomously.

3.4 Grounding Scheme

The whole NANOobc uses a single common ground topology. All parts of the NANOobc share a common ground. All connector pins with the signal type marked as GND refer to this common ground potential.

Additional ground signal types are:

- CAN ground: connected to GND through a 0 Ohm resistor near the CAN driver.
- LVDS shield: connected to GND through a 0 Ohm resistor near the LVDS driver.

3.5 Electro Static Discharge

The NANOobc contains sensitive electronic components that are susceptible to be damaged by static electricity. When handling or installing the NANOobc observe appropriate precautions and ESD safe practices.

3.6 Electromagnetic Compatibility

Each NANOobc can be upon request RF characterised and tested for EMC, according to ECSS-E-ST-20-07C. Tests are performed in facility certified for CCA EMC test procedures.

3.7 Mechanical Interface Control Drawing

The NANOobc is fully compliant to PC104 mounting specifications. For standard details please refer to RD2. NANOobc electronics board is fixed into common PC/104 compliant fixation rod. Cable stripes are used to provide power and establish communication link between NANOobc and other command and data handling equipment, over CAN and high speed LVDS interfaces.

Please take special care when designing mechanical stack up, to keep clear of exposed components of the NANOobc subsystem. It is recommended to provide a clearance between this and another component in stack up of at least 2 mm on top and bottom.

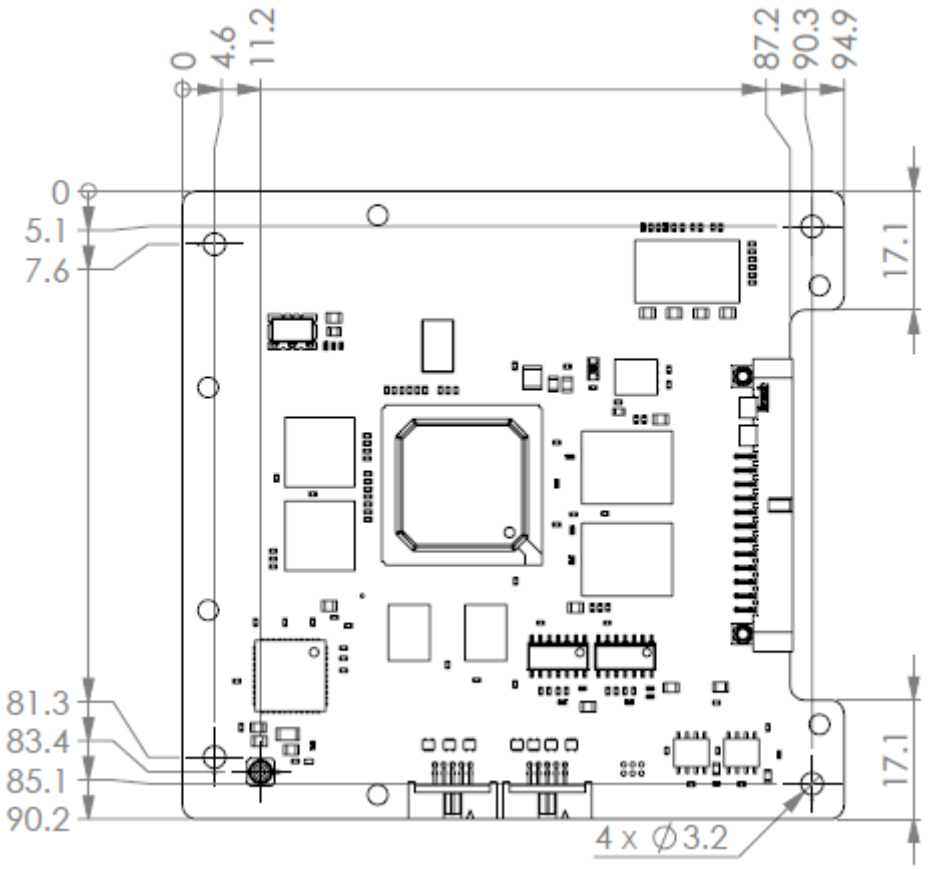

Figure 5: Mechanical Drawing of NANOobc – Top view

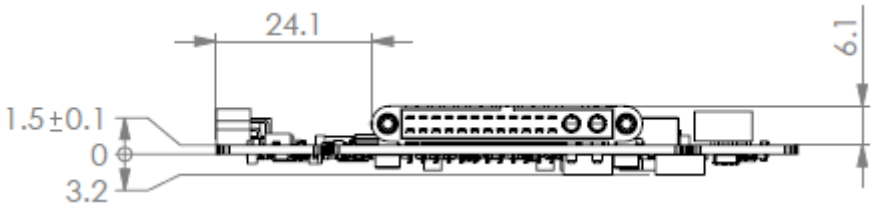

Figure 6: Mechanical Drawing of NANOobc – Front view

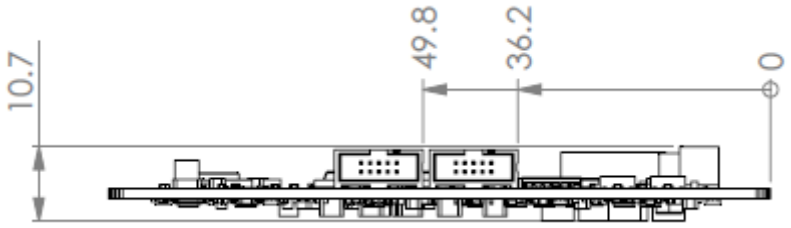

Figure 7: Mechanical Drawing of NANOobc – Side view

3.8 Mechanical Interface Control parameters

NANOobc mechanical properties:

Table 5: NANOobc mechanical properties:

Dimensions:	90.2 x 94.9 x 10.8 mm (92.45 cm³)
Mass:	54.00 g (PCB, components) – unmargined 55.05 g (PCB, components) – 5% margined

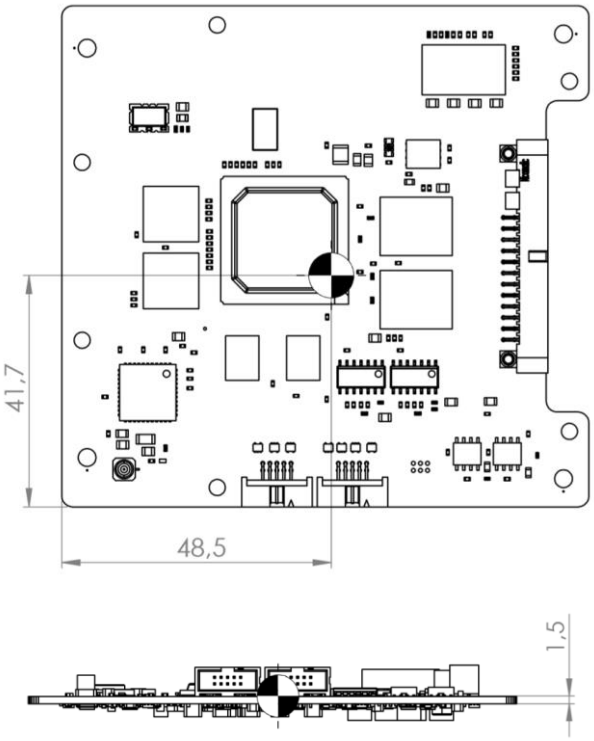

Figure 8: Centre of mass

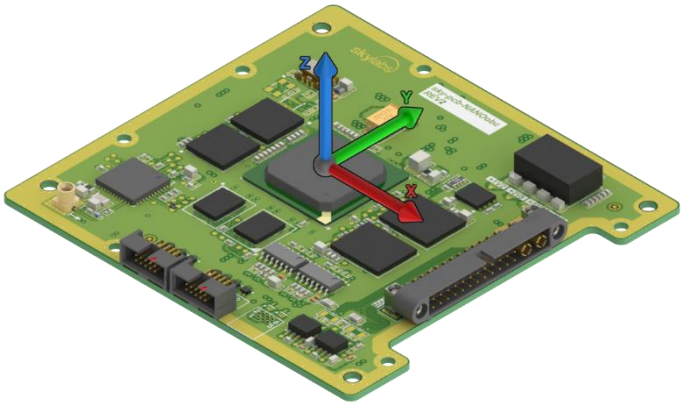

Figure 9: Reference coordinate system

Moments of inertia: (grams * square millimeters)

Taken at the centre of mass (Figure 8) and aligned with the output coordinate system (Figure 9).

Table 6: NANOobc moments of inertia

Lxx = 40242.27	Lxy = 3314.99	Lxz = 241.36
Lyx = 3314.99	Lyy = 30825.67	Lyz = -726.67
Lzx = 241.36	Lzy = -726.67	Lzz = 70750.95

3.8.1 Materials specifications

Material	Manufacturer	%TML	%CVCM	%WVR	Application	Note
PCB material	ISOLA 370HR			0.15	PCB board	ECSS identified
Solder	Indium 8.9HF1				Soldering	

3.8.2 List and location of thermal sensors

Sensor	Name	Type	PCB location
T1	FPGA Sensor	External NTC (B=3380)	Bottom
T2	Regulator Sensor	Internal Sensor of Power Regulator	Top

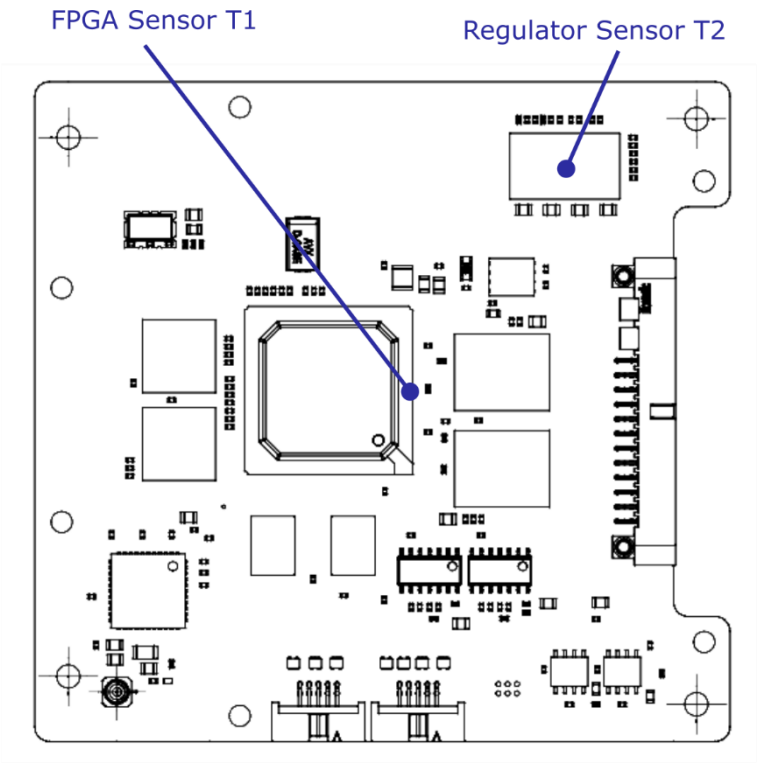

Figure 10: Location of NANOobc Thermal Sensors

3.9 Environmental Requirements

3.9.1 Thermal Limits

Table below describes the thermal limits for the NANOobc. Recommended values for all electronic modules are provided in the table.

The definition of the Design, Acceptance and Qualification limits are as follows:

- **Design Temperature**: The temperature to which the flight equipment can operate in service and work satisfactorily.
- **Qualification Temperature**: The temperature to which the module design has been tested and proven to work satisfactorily.

- **Acceptance Temperature**: The temperature to which the flight equipment has been tested and proven to work satisfactorily.

Table 7: Temperature Limits

	Qualification	Acceptance	Design
Non-operating temperature limits	-30°C - +75°C	-25°C - +70°C	-20°C - +65°C
Start-up temperature limits	-35°C - +70°C	-30°C - +65°C	-25°C - +60°C
Operating temperature limits	-20°C - +70°C	-15°C - +65°C	-10°C - +60°C

3.9.2 Thermal Dissipation

This section provides information on the thermal dissipation of the NANOobc modules, in Watts.

Thermal dissipation will be less than estimated power consumption for each module.

Table 8: NANOobc Power Dissipation

	Power Dissipation [W]	Primary thermal path
NANOobc	< 1 W	To PCB fixation holes

3.9.3 Definition of External Surface Properties

NANOobc module is not incorporated into any enclosure.

4 Harness

NANOobc provides power and separate communication interfaces connector.

4.1 NANOobc connectors

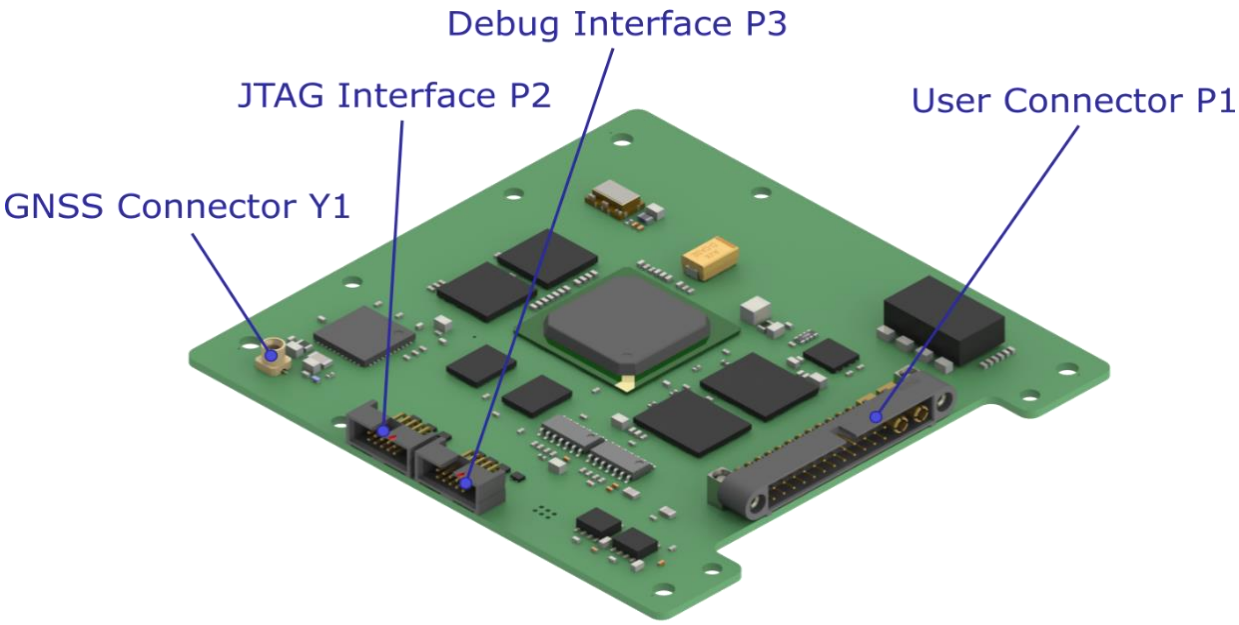

Figure 11: NANOobc connector designators

4.1.1 User connector

Connector name:	**NANOobc Power and Communication connector**
Connector designator:	**P1**
Connector function:	**Power supply and communication interface**
Connector type:	**Multi-mix connector, power and signal to the Board, MALE**
Connector part number:	**221V24F26-0200-3400CMM**
Mate connector part number:	**222S24M16-0200-4310**

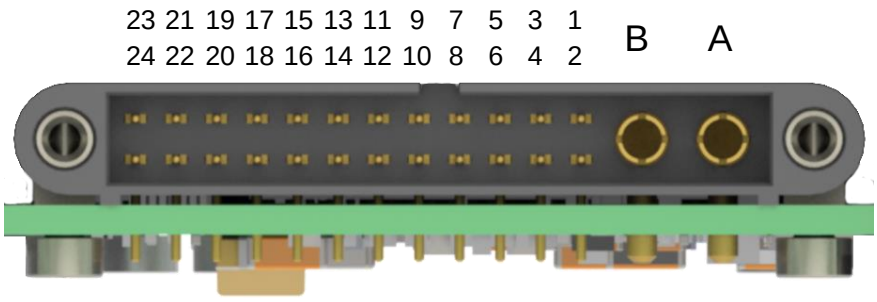

Figure 13: NANOobc Power and Signal Connector (221V24F26-0200-3400CMM)

Table 9: NANOobc Power and Signal connector pins (221V24F26-0200-3400CMM)

Pin	Signal Name	Signal Type	Wire Type	Notes
A	Power +5V	+5 V power supply	AWG-16	
B	Power GND	GND	AWG-16	
1	CANB_P	CAN signal level	AWG-26	Redundant bus
2	CANB_N	CAN signal level	AWG-26	Redundant bus
3	CANB GND	CAN ground	AWG-26	Redundant bus
4	CANA GND	CAN ground	AWG-26	Nominal bus
5	CANA_P	CAN signal level	AWG-26	Nominal bus
6	CANA_N	CAN signal level	AWG-26	Nominal bus
7	LVDS1_SHD	LVDS TX cable shield	AWG-26	
8	LVDS0_TX_P	LVDS signal level	AWG-26	
9	LVDS1_TX_P	LVDS signal level	AWG-26	
10	LVDS0_TX_N	LVDS signal level	AWG-26	
11	LVDS1_TX_N	LVDS signal level	AWG-26	
12	LVDS0_RX_N	LVDS signal level	AWG-26	
13	LVDS1_RX_N	LVDS signal level	AWG-26	
14	LVDS0_RX_P	LVDS signal level	AWG-26	
15	LVDS1_RX_P	LVDS signal level	AWG-26	
16	LVDS0_SHD	LVDS TX cable shield	AWG-26	
17	GPIO7	GPIO	AWG-26	GPIO0_7
18	GPIO6	GPIO	AWG-26	GPIO0_6
19	GPIO5	GPIO	AWG-26	GPIO0_5
20	GPIO4	GPIO	AWG-26	GPIO0_4
21	GPIO1_P	GPIO / LVDS Differential	AWG-26	GPIO0_1
22	GPIO1_N	GPIO / LVDS Differential	AWG-26	GPIO0_1
23	GPIO0_P	GPIO / LVDS Differential	AWG-26	GPIO0_0
24	GPIO0_N	GPIO / LVDS Differential	AWG-26	GPIO0_0

4.1.2 NANOobc GNSS RF Connector

Connector name: **NANOobc GNSS RF connector**

Connector designator: **Y1**

Connector function: **RF**

Connector type: **50 Ohms, SMPM Plug, PCB Mount, Vertical**

Connector part number: **73300-0080**

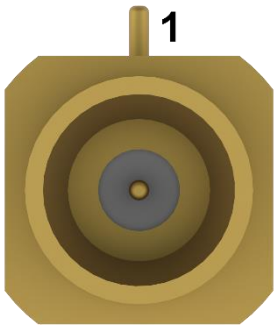

Figure 12: NANOobc RF Connector (73300-0080)

5 Telecommands and Telemetry

This section is left empty, for NANOobc is delivered without complete on-board software. However, RTOS environment with peripheral drivers is delivered in any case.

6 Interfaces - Electrical Characteristics

6.1 CAN interface

Controller–area network (CAN or CAN-bus) is an automotive bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer. CAN is a message-based protocol, designed specifically for automotive applications but is now also used in other areas, such as industrial automation, medical equipment, and for space applications.

CAN is a multi-master broadcast serial bus standard for connecting Electronic Control Units (ECUs). Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an id, which represents the priority of the message, and up to eight data bytes. It is transmitted serially onto the bus. This signal pattern is encoded in Non-Return-to-Zero (NRZ) and is sensed by all nodes.

The devices that are connected by a CAN network are typically sensors, actuators, and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.

If the bus is free, any node may begin to transmit. If two or more nodes begin sending messages at the same time, the message with the more dominant ID (which has more dominant bits, i.e., zeroes) will overwrite other nodes' less dominant ID's, so that eventually (after this arbitration on the ID) only the dominant message remains and is received by all nodes. This mechanism is referred to as priority-based bus arbitration. Messages with numerically smaller values of ID have higher priority and are transmitted first.

NANOobc TM/TC is based on CAN Specification (RD1), Version 2 Bosch GmbH – CAN standard B, 29-bit Identifier, at the application layer the CAN-TS protocol is delivered, developed by SkyLabs.

The CAN standard requires that the CAN bus is terminated at each end by a one-hundred-and-twenty-ohm (120 Ohm) resistor. It is possible that the termination resistors are fitted in the harness/connector and not in the module.

6.1.1 CAN Physical Interface

6.1.1.1 CAN Physical Interface electrical specifications

Table 10: CAN Interface electrical specifications

Parameter	Minimum	Typical	Maximum
Maximum DC voltage	-58V	N/A	58V
Maximum transient voltage	-150V	N/A	100V
Maximum current	-40mA	N/A	100mA
ESD discharge (HBM) *	- 8kV	N/A	+8kV
ESD discharge (IEC 61000-4-2) *	- 8kV	N/A	+8kV
* Discharge at available pins CANH and CANL on connector			

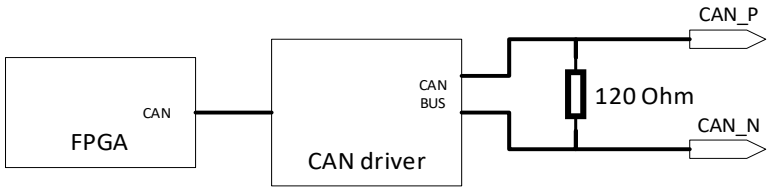

Figure 13: CAN interface schematic (note: 120 Ohm termination resistor optional)

6.1.2 CAN Redundancy Operation

NANOobc support communication over cold or hot redundant CAN busses. In case hot redundant networking topology is not considered in satellite, hot redundant operation can be disabled.

Hot redundant operation means that transmitting CAN node transmits single frame throughout both CAN busses concurrently. Receiving CAN nodes are listening on both CAN busses, where receiving CAN arbiter selects bus, on which the CAN frame arrived first. In case of detecting concurrent reception, arbiter always select primary CAN bus (CAN_A).

6.2 LVDS Interface

TM/TC communication is performed via the hot-redundant CAN bus. The CAN bus is sufficiently fast for TM&TC purposes but for high data rate transmission over RF a dedicated high-speed link is provided.

In order to implement this high-speed data link, a LVDS interface is chosen. It requires a double differential pair signal cable, one for each way, allowing full-duplex high-speed data transfer. Differential drivers and receivers meet or exceed the requirements of the ANSI TIA/EIA-644-1995 standard.

6.2.1 LVDS Physical Interface

The LVDS interface can provide data rates up to 20Mbps while bus-terminal ESD exceeds 12 kV and operates in wide temperature range. Selected LVDS physical driver is intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state, but rather disconnects the input and reduces the quiescent power used by the device.

6.2.1.1 LVDS electrical specifications

Table 11: LVDS driver electrical specifications

Parameter	Minimum	Typical	Maximum
Differential output voltage	247 mV	340 mV	454 mV
Change between differential output voltage	-50 mV	NA	50 mV
Steady-state common-mode output voltage	1.125 V	1.2 V	1.375 V
Peak to peak common-mode output voltage	NA	50 mV	150 mV

Table 12: LVDS receiver electrical specifications

Parameter	Minimum	Typical	Maximum
Positive-going differential input voltage threshold	NA	NA	100 mV
Negative-going differential input voltage threshold	-100 mV	NA	NA
High level output voltage	2.4-2.8 V	NA	NA
Low level output voltage	0.4 V	NA	NA

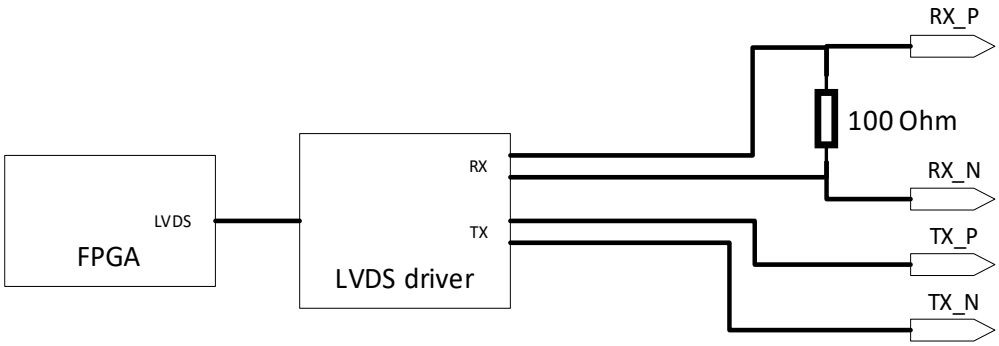

Figure 13: LVDS interface schematic

6.3 GPIO interface

The GPIO interfaces feature general purpose I/Os with I/O remapping capability (capability to use GPIO pins for alternative functions, such as PWM, UART, I2C, SPI, etc.). The GPIO interface follows the LVCMOS 3.3V standard or LVPECL if GPIOs are configured as differential signal pair with on-board resistor termination.

All GPIO pins are connected to FPGA I/O pins, with a 10 Ohm resistor in series.

Table 13: GPIO interface electrical specifications

Parameter	Minimum	Typical	Maximum
Input current	N/A	N/A	10 uA
DC Input High	2.0 V	N/A	3.45 V
DC Input Low	-0.3 V	N/A	0.8 V
Output current	N/A	N/A	12 mA
DC Output High	2.9 V	N/A	3.3 V
DC Output Low	0.0 V	N/A	0.4 V
In-series resistance	N/A	10 Ohm	N/A

Table 14: GPIO interface electrical specifications (differential LVDS configuration)

Parameter	Minimum	Typical	Maximum
Input current	N/A	N/A	10 uA
DC Input Limits	0.0 V	N/A	2.925 V
Differential output voltage swing	0.25 V	0.35 V	0.45 V
Output common mode voltage	1.125 V	1.25 V	1.375 V
Input common mode voltage	0.05 V	1.25 V	2.35 V
Input differential voltage	0.10 V	0.35 V	0.60 V
Output current	N/A	N/A	12 mA
DC Output High	1.25 V	1.425	1.6 V
DC Output Low	0.9 V	1.075	1.25 V

Termination resistance	N/A	100 Ohm	N/A

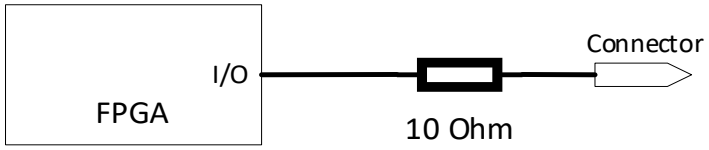

Figure 13: GPIO connection schematic

6.4 FPGA JTAG Interface

JTAG interface is available on NANOobc. The JTAG interface (P3) is used for flashing FPGA configuration. The JTAG interface is compliant to the standard 10-pin connector and can be used in conjunction with proprietary software provided by the FPGA manufacturer. The signal levels for the terminal interface are CMOS 3.3V.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

6.5 PicoSkyFT Processor Debug interface

The NANOobc uses a dedicated Debug interface (P4) for accessing the embedded soft-core processor PicoSkyFT. Using a proprietary protocol and an PicoSky-Link programmer provides unified access to the internal registers of the processor, to all internal and external memories, and to all peripheral units of the NANOobc. The signal levels of the PicoSky Debug interface are compliant with CMOS 3.3V levels. This interface is used for the firmware downloading to the NANOobc's non-volatile memories. Furthermore, this interface provides unified debugging of the downloaded software using standard GNU (gcc, gdb) toolchain and propriety PicoSky-gdbproxy server.

NOTE: Do not use interface without SkyLabs approval, instruction and relevant equipment.

A. Appendix A

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