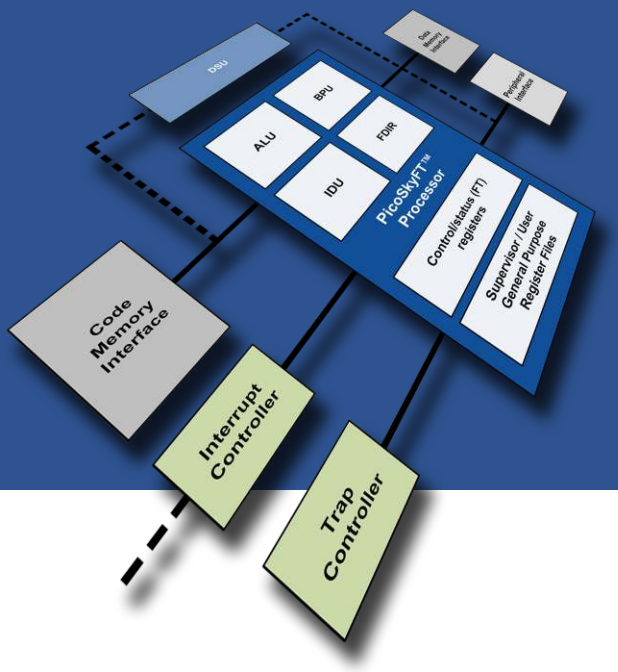
PicoSky™ Fault Tolerant processor

Small footprint 8/16 bit soft-core processor



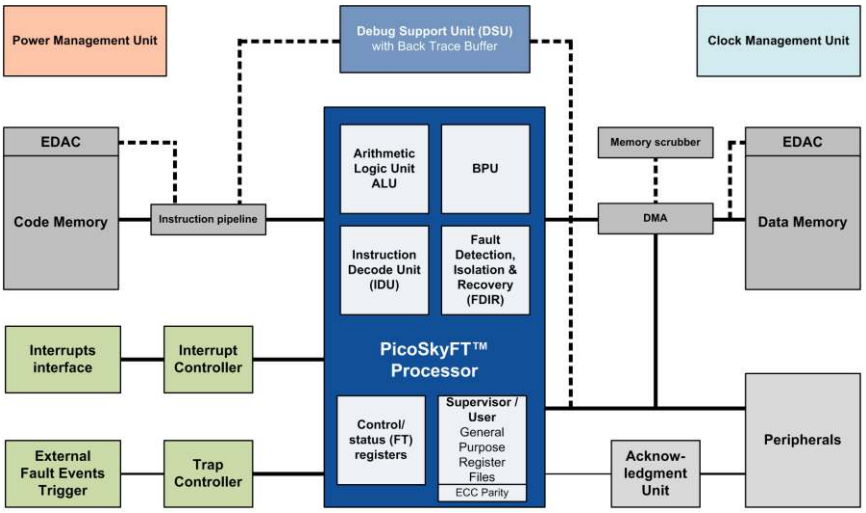
Description

PicoSkyFT™ is designed for embedded processing functions within System on Chips by providing another layer of abstraction to tackle complexity and adequately respond to rapidly changing needs, and securing development and verification efforts. Rad hard by design, small size, low power and configurable architectural features optimised for hard, real-time processing make this type of core suitable for multi-core specialised applications. The PicoSkyFT™ is a high performance Fault Tolerant 8/16-bit embedded processor based on Harvard enhanced RISC pipelined architecture designed to provide a next generation solution that fits between the overloaded FPGAs and the hugely complex microprocessors. The processor provides a rich and powerful instruction set with 16-bit operation codes with single cycle execution on most instructions to provide throughputs of 1 MIPS per MHz. The SEE tolerant design is achieved by several error mitigation techniques and incorporated fault detection, isolation and recovery policy to increase reliability. The core is customisable to suit various memory models.

PicoSky™ ***class***	RISC	*Fault Tolerant*	FDIR	EDAC	SEU/T **tolerant**

PicoSky™ Fault Tolerant soft-core processor

Block diagram



Features

- PicoSky Fault Tolerant High performance 8/16 bit architecture
  - Harvard enhanced RISC pipelined architecture
  - Operating in five distinguished modes
  - Supervisor mode (privilege instructions execution, traps handlers)
  - User mode (restricted instruction set, interrupts handlers) Debug, Sleep, and Reset mode
- Radiation hardened by design
  - All memories EDAC protected
  - Several EDAC algorithm schemes available (Multiple SEC-DED)
  - EDAC/parity protected supervisor and user register files
  - Trap handlers invoked in case of detected faults
  - MR ready on register, module, and/or core level (PicoSky™ TRIcore)
  - Traps Controller
  - Handles several mitigated fault sources - traps for accomplishing FDIR policy
  - User defined FDIR policy for each trap respectively
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- Program memory addressable up to:
  - PicoSky-Basic version: up to 8 KB
  - PicoSky/FT-PRO version: up to 8 MB
  - Configurable supervisor/boot section size
- Data memory addressable up to:
  - PicoSky-Basic version: up to 64 KB
  - PicoSky/FT-PRO version: up to 16 MB
- Configurable Interrupt Controller
  - Customisable number of interrupt vectors
  - Prioritised interrupt vectors
- Debug and Test Facilities
  - Debug Support Unit (DSU) for Trace and Debug
  - Advance Debug interface
  - Configurable number of hardware watchpoints
- Software support
  - GNU GCC tool chain
  - GDB debugging support for complete core manipulation
  - PicoSkySim™ cycle exact processor simulator
  - Macro-based assembler available for low level software design
  - Software debugger supporting complete core manipulation
  - FreeRTOS supported
- System-On-Chip Design
  - Versatile Peripheral Interface

Deliverables

- PicoSky/PicoSkyFT™ soft-core RTL in Verilog HDL
- Test bench in Verilog HDL (covers 100% of instruction set)
- Reference design with pre-synthesis, post-synthesis, post layout, and physical design simulations
- Complete SDK (Linux and Windows OS)
- PicoSky Evaluation / development board (dev-picosky-a3pe3000 or -m2gl050)
- PicoSkySim™ C-library and demo example
- Software examples

Part number

- PicoSky-Basic soft-core picosky-basic
- PicoSky-PRO - soft-core picosky-pro
- PicoSkyFT-PRO - soft-core picosky-ft-pro